EE 307 MT RVW

**Transistors**

Why MOSFETs are competitive or better than BJTs now

* MOSFETs are easier to automate and design with because I**gat**e=0 whereas I**base** ≠0.
* Power
* Loading
* MOSFETs are easier to fabricate (= cheaper)
* MOSFETs give more options for low voltage design.

**Why BJTs have an edge when the same size as MOSFETs**

* **Current equation for BJT is exponential; for MOSFET is quadratic**
* **dv/dt = I/C**
* **But MOSFETs drop capacitance**

Be able to draw a cross section and top view of MOSFETs and BJTs and label capacitances and terminals

What abstraction is

What PN junctions are on and off in a MOSFET during operation. For MOSFETs, all junctions are turned off Made not to conduct.

Know why you need to connect a substrate to the correct voltage (NMOS substrate to lowest voltage in system, PMOS to highest voltage in system)

So you can pull up and pull down from there

Why NMOS can’t be pullup and why PMOS can’t be pulldown: doesn’t go rail to rail, goes into cut off before then

**for the same sized devices, generally, N devices conduct more and have a steeper IC/IDS vs VBE/VGS curve because of their higher mobility**

Channel-length modulation (MOSFET - 1 + lambda VDS) and base-width modulation (BJT - 1+ (VCE/VA))

**Simulation**

**DC sweep (Sweep something other than time. R, V, I… That is what will be on the X-axis. Sets value on input and does DC bias point simulation. Sets another value and does DC bias point simulation. Though it looks like a signal is moving, because each measurement is done at DC values, C acts as open circuit and L as a short. NOT A time related MOVING SIGNAL!)**

**What a .op (or DC bias point) simulation is: DC bias point (.op) puts DC value on input and, after everything settles tells you what the node voltages are and what branch currents are for that SINGLE DC input**

**Model file: a description from the fabricator on how a particular device works so you accurately simulate your circuit before it’s actually fabricated**

What happens if you don’t use a model file (where does LTSpice get its values from if you don’t specify them)

PWL (Piece-wise linear) inputs: a way to set the input to your circuit.

**Why you need symbols :Only way to make large designs by hand is re-use and the use of hierarchy.**

Two ways to include model information (text file and manual writing)

**Rwire = RSQR \* L/W**

**C = area \* C per unit area**

**CMOS**

POS

**IC design:**

**Know that many chips are built by writing some Verilog or VHDL and then letting the software automatically create a chip for you. Turning an HDL into gates is called synthesis and drawing the gates into silicon is called place and route.**

**Know that the majority of those chips use CMOS as their logic family.**

**Load lines and the VTC**

i) Load lines to visually find operating point for voltage divider

ii) Load lines to visually find operating point for RTL

iii) Load lines to visually find operating point for CMOS inverter

iv) Voltage dividers

v) VTC: Transfer characteristic graph:

current on one or both of the axis. In general, the transfer curve has input on the X-axis (current or voltage) and output on the Y-axis (current or voltage). In this class we’ll be almost 100% V vs V).

(2) Know where the good digital regions are and where the bad regions are. (1s and 0s)

(3) Know that a steep transition region is good because it makes the circuit regenerative (4) Know that a steep transition region may mean less drive current (why?) and a slower tp.

VTC has nothing to do with current

(5) Know that a steep transition region can mean less short circuit current power

**Circuits**

**Capacitance table??? On equation sheet**

xii) Know which capacitance changes when region of operation changes and which don’t (CGC changes. The rest don’t)

xiii) How to find R (4 ways) for a transistor. (The R for the delay equations)

(1) Know how to find effective R for a graph using single point (3/4 Vswing)

(2) Know how to find effective R for a graph using two points (average of 1/2 Vswing and Vswing)

(3) Know that you can find R using integration but no need to know the math

(4) Know how to find R if I give you (k’/2)(W/L)

xiv) Dynamic metrics: tpHL, tpLH, tr, tf (delay & speed)

xv) Delay: Know the definitions for propagation (Vin=50% to Vout=50%), rise (Vout=10% to Vout=90%)

and fall (Vout=90% to Vout=10%) time.

(1) Know that delay is based on RC time constants

(2) Know how to use the equations for RC curves:

(3) Know tr=2.2RPMOSC, tf=2.2RNMOSC

(4) tp=0.69RC

(5) Know how to set up the equations to find the delay between two voltages

(6) Know that there is a second tp equation:

**Power:**

(2) Know when short circuit power dissipation occurs

(3) Know equation for dynamic energy for one transition

(4) Know that leakage occurs when devices are in cutoff but still leak some current

(5) Know that power is only dissipated on low to high transitions. Power is only used when current is

pulled off of the supply.

(6) Power including probability

xvii) Know what static power is (RTL, pseudo NMOS etc experience this)

xviii) Energy of a transition of a single inverter (C\*Vdd2)

**xix) Know that there is usually a tradeoff between power and speed**

**Voltage Controlled Oscillator**